Synchronization of transient digitizers to random events

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A circuit is described which synchronizes the timebase of a transient waveform digitizer to a randomly occurring trigger signal synchronous with the experiment information which is to be digitized. The method described overcomes the triggering ambiguity of the recorder and, therefore, uncertainties in time origin of the recorded signals. Pretrigger information is still preserved accurately except for a ± 1 sample period uncertainty prior to the trigger event. The design is based around a 200-MHz sample rate digitizer and uses a clock generator, which can be synchronized within one period to an external event. The same technique is applicable to slower clock rates and up to ~ 500 MHz.

INTRODUCTION

In recent years, high-speed transient digitizers have been increasingly used to capture single-shot analog waveforms in a variety of experimental situations. They have considerable advantages over storage oscilloscopes particularly because they offer the possibility of storing information prior to the triggering point. Two types of instruments are commonly used: those relying on an electron beam writing on a target which is subsequently read by a slower electron beam and those relying on a fast analog-to-digital converter followed by a memory.

The first type of instrument (e.g., Tektronix 7912D, 7250) enables subnanosecond sampling intervals to be achieved and the synchronization circuit described here could not be applied to them; in any case, their high sampling rate is sufficient to capture accurately fast events in most applications. The second type of instrument, which relies on a clock to determine the sampling interval, is available with typically maximum sampling rates of 20–500 MHz, i.e., 50–2-ns sampling interval (e.g., Biomation 8100, 6500, Tektronix 7612D) or more recently with 1.3-GHz sampling (LeCroy 6880). These devices have the drawback that the phase of the clock is inherently unsynchronized to an incoming random event and, hence, the ultimate time resolution cannot be utilized since there will be a $\pm$ 1 clock pulse maximum jitter on the stored waveform.

In many cases the arrival time of the input event can be predicted and arrangements have been applied to use the digitizer clock to generate the event at a fixed time later.[1] However, in some applications, such as in pulse radiolysis experiments using high-energy electron pulses[2] the input event time cannot be predicted. The problem is particularly serious in installations such as that in our laboratory where the pulsed radiation source is a Van de Graaff accelerator which uses a mercury-wetted coaxial reed relay[3] to inject a nanosecond electron bunch into the accelerating tube. An analogous situation occurs in installations which use a Febetron as the radiation source. The circuit arrangement described here can be used to overcome this limitation and ensures synchronization of the digitizer clock within two clock periods. If the input signal is delayed by, say, four clock periods an accurately synchronous stored replica of the input waveform will be obtained. Pretrigger information is still captured with this system, albeit with a short, variable break ahead of the principal event; in most cases this limitation is insignificant and the input signal delay is readily achieved using coaxial delay lines. In many situations this delay may already be inherent in the detectors and amplifiers used in the experimental setup.

I. METHOD

A diagram of the synchronization system is shown in Fig. 1 and is based around a Tektronix 7612D digitizer (5-ns sample rate). In our application we are interested in measuring changes in optical absorption or electrical conductivity in solutions irradiated by a short, variable amplitude and high-energy electron pulse. The electron pulse is passed through a single-turn toroidal ferrite transformer which provides a suitable trigger signal.[4] In many cases a trigger signal can be obtained with a simple loop near the irradiated sample instead of the toroidal transformer. This signal (<1-ns rise time) is a reasonable replica of the electron pulse shape and is, therefore, variable in both amplitude (10 mV–50 V) and duration (1.5–100 ns) depending on the particular experiment. This signal is shaped by two limiting amplifiers to generate a step lasting for ~ 100 ns. This step is converted into a 4-ns constant amplitude pulse, by using a shorted stub 2 ns long in parallel with the limiter output,[5] synchronous with the beginning of the radiation pulse. The leading edge of this pulse is used to turn off an oscillator while the trailing edge is used to restart it. It is essential to ensure that the oscillator can be turned on rapidly and that the first and subsequent periods after turn on are identical. In other words an oscillator with a rapid settling time is required; in our case a 200-MHz oscillator is needed to provide the necessary digitizer clock. It should be pointed out that since the clock oscillator is running before the trigger input the digitizer can capture pretrigger information and the uncertainty in the synchronizing time is only present during the 4 ± 5-ns

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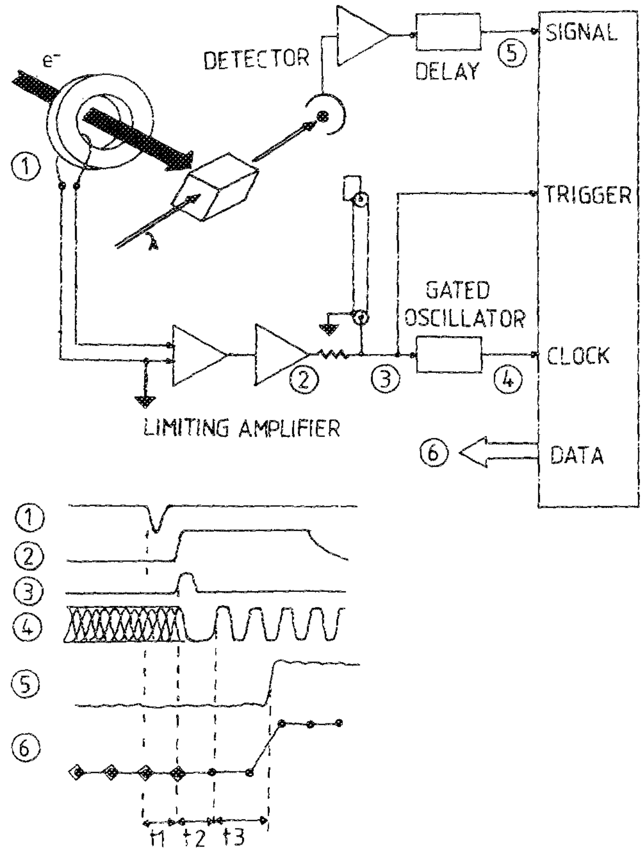

FIG. 1. Principle of operation of synchronizing circuit. A trigger signal (1) is shaped to produce the digitizer trigger pulse (3); t_1 is a delay introduced by the limiting amplifiers. The gated oscillator is synchronized (4) to the falling edge of (3) and the digitizer takes its first "correct" sample at times $t_1 + t_2$. The signal information (5) is delayed by $t_1 + t_2 + t_3$ and is digitized (6); the time at which the sampled points shown in squares are taken is indeterminate, but all subsequent samples are synchronized to (1).

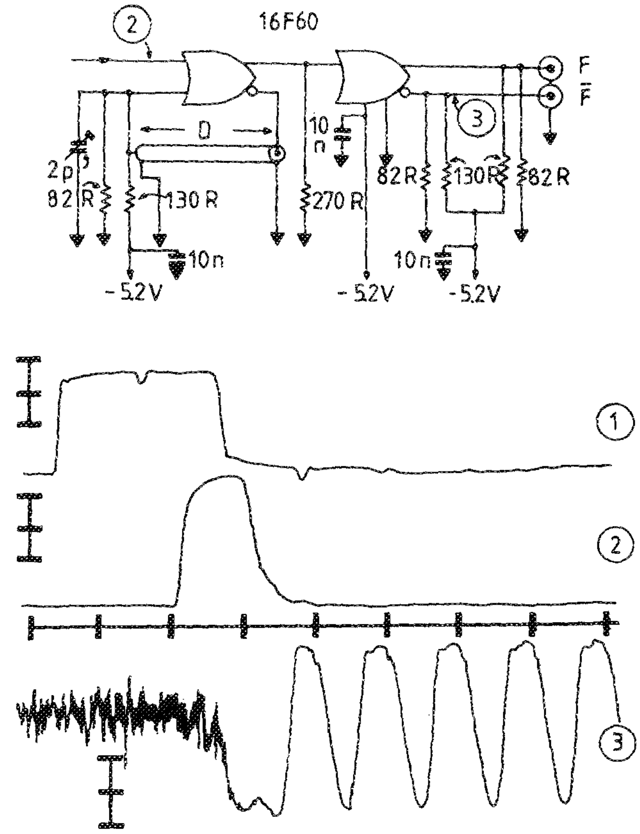

FIG. 2. The gated oscillator circuit using a dual four-input OR–NOR ECL gate. Oscillation period is determined by the delay line D, terminated by R_1, R_2; C is used to trim the total circuit delay. The second gate is used to buffer the output of the oscillator; all unused inputs are left open circuited. The oscillograms in the lower half of the figure are taken at 5 ns div^{-1} (1) 2 mV div^{-1}, input trigger signal; (2) 200 mV div^{-1}, oscillator gating signal; (3) 200 mV div^{-1}, oscillator output.

period of the gating pulse. When the clock oscillator is gated on, it is synchronized to the leading edge of the trigger pulse, i.e., to the beginning of the radiation pulse. Since the signal is delayed by typically four clock periods, i.e., 20 ns, the first signal sample is always acquired at the same, constant time following the onset of the trigger event. Ultimately the sampling aperture uncertainty of the digitizer analog-to-digital converter will limit the jitter in the acquired waveform. The aperture uncertainty in this case is ~ 100 ps and is, therefore, negligible for all practical purposes.

The gated oscillator is the most critical part of the system. Oscillators which rely on a tuned circuit (LC, quartz crystal or resonant line) usually show a trade-off between frequency stability and settling time and the author was not successful in applying these for the present purpose. Nevertheless, a particularly simple digital oscillator, which uses a delay line to determine operating frequency can be used in this application. This is shown in Fig. 2. The upper frequency of oscillation is in excess of 500 MHz if high-speed emitter-coupled logic (ECL) is used; this is limited by the propagation delay in the gate and could be increased by using gallium arsenide logic which is becoming available. The oscillation period is given by twice the sum of the transit times of the delay line and gate and it is, therefore, necessary to discharge the delay line by at least a $\frac{1}{2}$ oscillator period when turning the oscillator off, hence, the 4-ns gating pulse used in this case. The frequency stability of such an oscillator is more than adequate for this application as the delay line transit time is to all intents and purposes constant and the gate propagation time is small (~500 ps). Variations in gate threshold levels with temperature and supply voltage can be made small by using a suitable stabilized power supply. The oscillation frequency can be adjusted over a small range by using a low-value (~1–2 pF) trimmer capacitor as part of the line termination; this in effect alters the line delay in conjunction with the inevitable interconnection lead inductances. In principle, the temperature stability can be improved by using a tuning capacitor which exhibits a suitable temperature coefficient and cancels gate propagation delay variations. This was not felt to be necessary in the present application where a frequency stability of $< \pm 0.1\%$ could be readily achieved using the Plessey 16F60 ECL gate and a delay line made from RG178 cable. The second gate is used to buffer the oscillator and provides two complementary outputs, one of which is used to feed the digitizer clock input and the other is available for connection to a frequency meter for calibration purposes.

The limiting amplifiers at the trigger input can be conve-

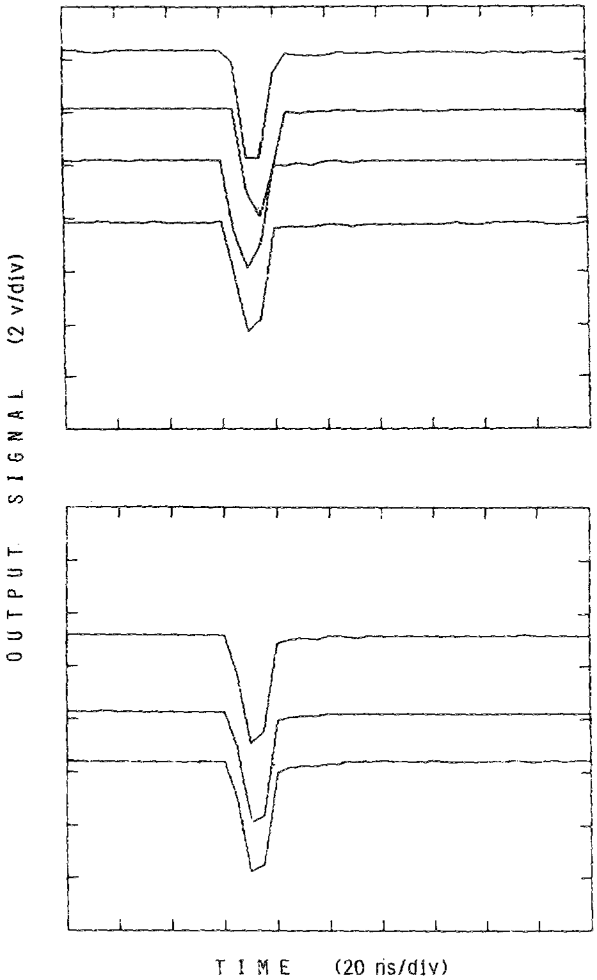

FIG. 3. Performance of the synchronizing circuit, used with Tektronix 7612D digitizer. The top traces are records of separate, nominally identical events (10-ns-wide pulses) acquired with the internal timebase of the digitizer; the effect of sampling uncertainty can be clearly seen. The lower traces (three separate nominally identical 10-ns-wide pulses) are obtained with the synchronizing circuit; any remaining uncertainty is due to the aperture time of the digitizer converter.

niently constructed using fast ECL comparators, Plessey SP 9680 which introduce a delay of ~5 ns in the trigger signal path; they have been found suitable for use with inputs down to ~2 mV with ~2-ns delay variations with a ×1000 overdrive. An additional delay ~3 ns is incurred due to the circuit layout. The total delay between the start of the trigger pulse and the first sample is thus ~16.5 ns.

In addition to the ECL trigger circuits, a TTL output is provided (10 μs–35 ns delay) which can be used to trigger auxiliary circuits and a monostable (~20 ms) which pulses a LED to indicate triggering of the circuit.

II. RESULTS AND CONCLUSION

The performance of the circuit is shown in Figs. 2 and 3. The oscillograms in Fig. 2 were obtained using a Tektronix sampling system, 7S11 vertical plug in with S2 sampling head and P6201 active probe, 7T11 sampling timebase. The detection rise time is < 200 ps. It can be seen that the oscillator is synchronized (trace 3) to the incoming trigger signal (trace 1) with a delay of ~16 ns. The oscillator is in fact running prior to the trigger event but, since it is unsynchronized to this event, the sampling system cannot capture the oscillator waveform which is displayed as noise.

In Fig. 2, the synchronizing system is used in conjunction with our Tektronix 7612D digitizer. In this case a 10-ns-wide pulse is applied to the digitizer; successive records obtained with the internal timebase of the digitizer show the effects of sampling uncertainty and the improvement due to the synchronizing circuit is clear. The circuit is particularly useful when several records are acquired for averaging or subtraction purposes; without timebase synchronization, the best obtainable time resolution in the final record would be degraded to ~10–15 ns compared to 5 ns with synchronization.

The oscillator was tested to 500 MHz using the 16F60 gate, but if ECL III logic is used (1660 gate) the maximum clock frequency is ~300 MHz. The total cost of the circuit is £~150; if one considers that this arrangement improves the effective time resolution attainable with a given digitizer by a factor of 2 this represents a worthwhile investment.

ACKNOWLEDGMENTS

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