A versatile peak detector: updated implementation of an old idea

1. Introduction

Some very simple, basic circuits are still going strong even after many decades. One of them is the active peak detector[1], sometimes called a peak-hold circuit, sometimes (incorrectly) called a full-wave rectifier. The peak detector does only one thing: it monitors a voltage of interest and retains its peak value as its output. The evolution of the classical approach, shown in Figure 1, is straightforward, though it is noted that care must be implemented on the right-hand diagram of Figure 1 to ensure that the combinations of the two amplifiers in the feedback path maintains an adequate phase margin. Strictly speaking, such peak detectors do not 'detect peaks' for example as with circuits that provide an output as to when a peak occurs, rather they provide an output equal to the peak value of a signal. Perhaps the original term for this type of circuit should have stuck: Precision peak reader and memory circuit…does not quite roll off the tongue but is indeed correct. Other approaches, such as designs based on digital signal processing[2], translinear approaches[3, 4], controlled current conveyor[5] or phase shifting approaches are not discussed here, since these are either complex, inaccurate, susceptible to high frequency noise, or more appropriately implemented in custom ICs or programmable devices.

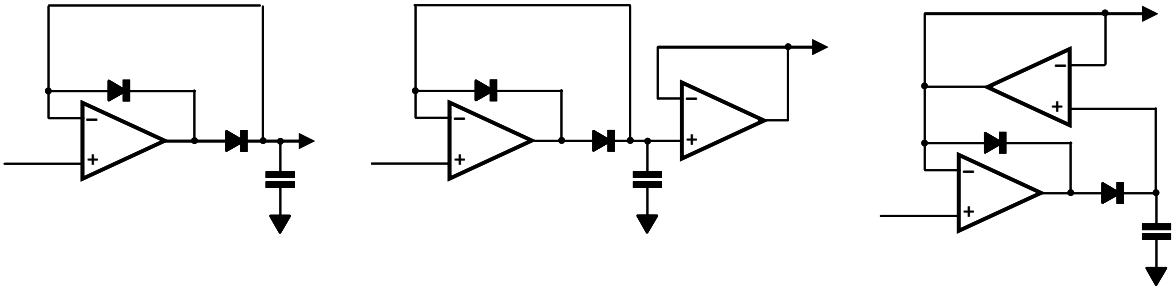

Figure 1: Evolution of the classical peak detector circuits, Left: single opamp circuit where the charging of the capacitor is performed by a series diode and the capacitor voltage is forced to follow the input voltage by the operational amplifier; discharge of the capacitor is defined by subsequent load. Middle: as in on left, but the capacitor output voltage is buffered by an output operational amplifier, isolating the capacitor from subsequent loads. Right: the 'buffer' output voltage is now sensed by the input amplifier which now no longer has to provide high input impedance. In all cases, a diode in the feedback path of the input amplifier restricts its negative-going output voltage swing.

The operation of these circuits is simple: the input amplifier charges the hold capacitor, and the diode prevents the capacitor from discharging. The input operational amplifier, in conjunction with the capacitor, presents that 'held' value as the output through the output operational amplifier. As the input voltage increases further, the capacitor is charged to the higher voltage; if the input voltage decreases below the previous value, the voltage on the capacitor stays at the previous peak value.

The purpose of this note is to describe in more detail some of the practical issues associated with this final (right-hand) circuit in Figure 1 and to provide details of a hopefully more versatile implementation of this circuit arrangement. Although many older readers are likely to have spent many a pleasant hour taming the vagaries of operational amplifiers from long ago, the same is true today, apart from the fact that modern high speed/high slew rate devices are much improved and thus easier to use. The variants of the designs presented here have all been tested and characterised.

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1 J. G. Graeme, G. E. Tobey, and L. P. Huelsman (Editors), OperationalAmplifiers, Design and Applications, McGraw-Hill, New York, 1971.
2 Implementing Accurate Peak Detection; Whitepaper by D. Sweet, Cypress Semiconductor Corp.
3 Translinear circuits: A proposed classification; B. Gilbert, *Electron Lett*, **11**, pp.14-16, 1975.
4 https://en.wikipedia.org/wiki/Translinear_circuit
5 A New Peak Detector Based on Usage of CCCIIs P.B. Petrović, 19th IMEKO TC 4 Symposium Advances in Instrumentation and Sensors Interoperability, 2013.

We had decided to develop a simple multipurpose printed circuit board when we found ourselves in the situation where we needed several such peak detectors in several instrumentation projects. We bit the bullet so to speak and describe a generic circuit arrangement for capturing peaks lasting for times of the order 50-2000 μs with the underlying assumption that the peak-detected output would ultimately be digitised. The basic analogue peak detector circuit requires just a few appropriately selected analogue components to capture and hold the signal's maximum value. Similar approaches were used long ago[6], when operational amplifiers were first developed. But as is often the case with analogue circuits, the devil is in the details.

2. Why not use a sample-and-hold?

Sample and hold circuits and peak detector circuits are closely related. Both use a capacitor as an analogue memory element. However, while this capacitor is connected to the driving circuit thorough a bidirectional analogue switch in the case of the sample-and-hold circuit, in the case of the peak detector, a unidirectional switch, a diode, is used for this purpose.

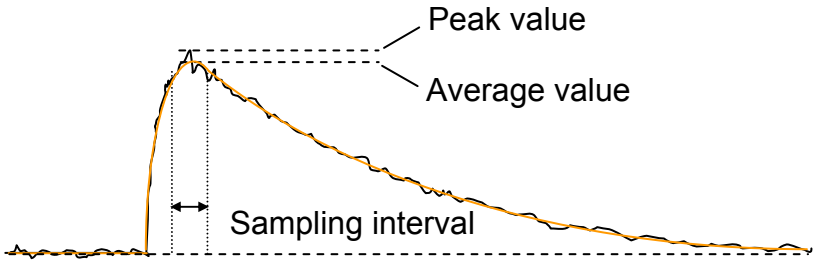

Figure 2: Differences between the peak detector and sample-and-hold circuits.

A sample-and-hold circuit requires a timing signal (the sample signal) to define the sampling interval as shown in Figure 2. In many cases, the timing of the input signal is unknown (e.g. when measuring a flashlamp output signal, a radiation detector output or similar) and then the question arises as to when to sample. In a synchronous arrangement, this may not be a problem, though a properly timed signal would of course be required. Other approaches rely on a comparator activated whenever the input voltage exceeds 0 V; such an approach can be found in the LM13700 transconductance amplifier data sheet[7]. It works just fine for slow rate of change signals.

Whether sampling or peak detector circuits are used, care must always be exercised when the input signal is noisy – as it almost always is. Clearly peak detector would not give optimal results when it 'sees' the noise peak. Low pass filtering should in general be used and optimised for the signal in question.

Why not just use a modern repetitively triggered analogue-digital converter, particularly one with an inherent sample-hold input circuit, based on charge redistribution successive approximation approaches? Well, we could of course have done that, but the burden would then be placed on (1) having enough storage space to handle the series of analogue-digital converter readings and (2) on software to sort them out in order to find the peak. It seemed easier to sort it out in the analogue domain. It is noted however, that in general, the approximate time of arrival of the peak is known to us (e.g. as in the flashlamp example above, or firing an accelerator or similar). When the arrival time of the input peak is not known at all, a software-based approach would indeed be not just essential but superior.

3. What limits performance?

The output voltage cannot change any faster than the time during which the capacitor in Figure 1 can be charged. The speed at which C is charged is limited by the short circuit output current of A1, the forward voltage drop of D1 and its commutation speed. Sometimes a resistor is placed in series with D1, in which case the exponential rise due the time constant formed by this resistor and C.

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6 Philbrick Applications Manual for Computing Amplifiers for Modeling, Measuring, Manipulating & Much Else 1966 , can be found at http://www.analog.com/library/analogdialogue/archives/philbrick/computing_amplifiers.html in the "Metering circuits" section (§III.50)

7 http://www.ti.com/product/LM13700

Clearly ensuring stability in Figure 1's right-hand circuit is essential and this is not always as straightforward as it seems at first sight. Approaches such as that described in an Analog Devices application note[8] break this outer loop and use compensation diodes. In the authors' experience such approaches are indeed fast but never perform particularly well at low input voltages. Nevertheless, the use of high current outputs from A1 is indeed valuable.

In the good old days we would not bother to write this note but would have been happy to use a self-contained chip, the PKD-01[9]. These were pretty expensive devices being thin film hybrid, peak-hold units[10], designed to track and hold the peak of analogue input signals with rise times (10% to 90% of Vmax) as short as 250 ns. Of course it does this at the expense of droop rate, spec'd to be as high 5V/sec at high temperatures. These devices are now obsolete and prohibitively expensive.

Another ugly issue that crops up regularly, at least in our work, is that the baseline level of the input signal is not always zero. For example if we are dealing with detecting the output from a system that has a zero offset on its output. Sure, we can trim this out to zero at a given temperature but this is not an elegant solution for ensuring long-term trust in the system operation. It would be good to clamp the input to true zero just before measuring the peak output.

4. Our design

Our design(s) are presented in Figures 3-6. These are all similar but use a range of semiconductor devices, in an effort to find the 'optimum'. Starting with the simplest design, shown in Figure 3, we start off by using a low pass filter (R1, C1) at the circuit input, providing a rise time of ~2.2 µs, i.e. a settling time of ~7 µs. Of course these values can be modified but should not be decreased too much. This time constant guarantees that there will not be any signal overshoot. Resistor R8 ensures that the input will not be open circuit but the arrangement is intended to be driven from a low impedance circuit. The charging amplifier U1 can be the venerable AD847 opamp. This is likely to become obsolete fairly soon but can readily be replaced by the ADA4637-1 as shown in Figure 5. The input offset compensation potentiometer is unlikely to be needed but has been included; note that different trimpot values are required for the two opamp types.

The opamp drives the peak storage capacitor C7 through R3 and diode D2: the FDH33 low leakage diode is useful for extending holding times but can equally well be replaced by a 1N4148 diode for more usual sub-second holding times (Figures 4 and 6). Resistor R3 limits the C7 charging/ discharge currents and provides a degree of protection for the opamp output circuits; some opamps will not need it. C7 is of course a critical component: any dielectric absorption here is detrimental. Ideally, a Teflon dielectric capacitor would be used here, but cost is extremely high and availability is, well, you try and find some in small quantities. More adventurous readers my wish to use Russian Teflon capacitors available through eBay, but lack of detailed specs is a bit of a problem. Good alternatives include polypropylene film capacitors, with a rated dielectric absorption of 0.05 to 0.1%, polyester film capacitors (0.2 to 0.5%) and polyphenylene sulphide film capacitors (0.05 to 0.1%). Interested readers should read articles on dielectric absorption (also called dielectric soakage) by B Pease[11] and others[12, 13].

We ended up using a small polystyrene capacitor (10 nF) for charge holding. An AD825 or ADA4627-1 FET amplifier is used to buffer the charge-hold capacitor. The AD825 is preferred for high speed applications, though its offset voltage is somewhat higher than the ADA4627-1. An ADG1201 switch is used for resetting purposes, providing a very low leakage when 'off' (<600 pA) and negligible charge injection (<1 pC) during reset. R5 and R6 are provided if the output voltage

8 https://www.analog.com/en/technical-articles/ltc6244-high-speed-peak-detector.html.
9 LM13700 Analog Devices PKD-01 https://www.analog.com/en/products/pkd01.html#product-documentation
10 Amptek Model PH300, http://amptek.com/products/ph300-peak-hold-detector/
11 www.electronicdesign.com/analog/whats-all-soakage-stuff-anyhow
12 www.keith-snook.info/capacitor-soakage.html
13 Ken Kundert Modeling Dielectric Absorption in Capacitors *www.designers-guide.com.*

needs to be attenuated (e.g.0-+5V as used by many current analogue-to-digital converter chips). For higher output voltages, modify accordingly, though some resistance at the output is desirable to isolate the circuit form subsequent large load capacitances.

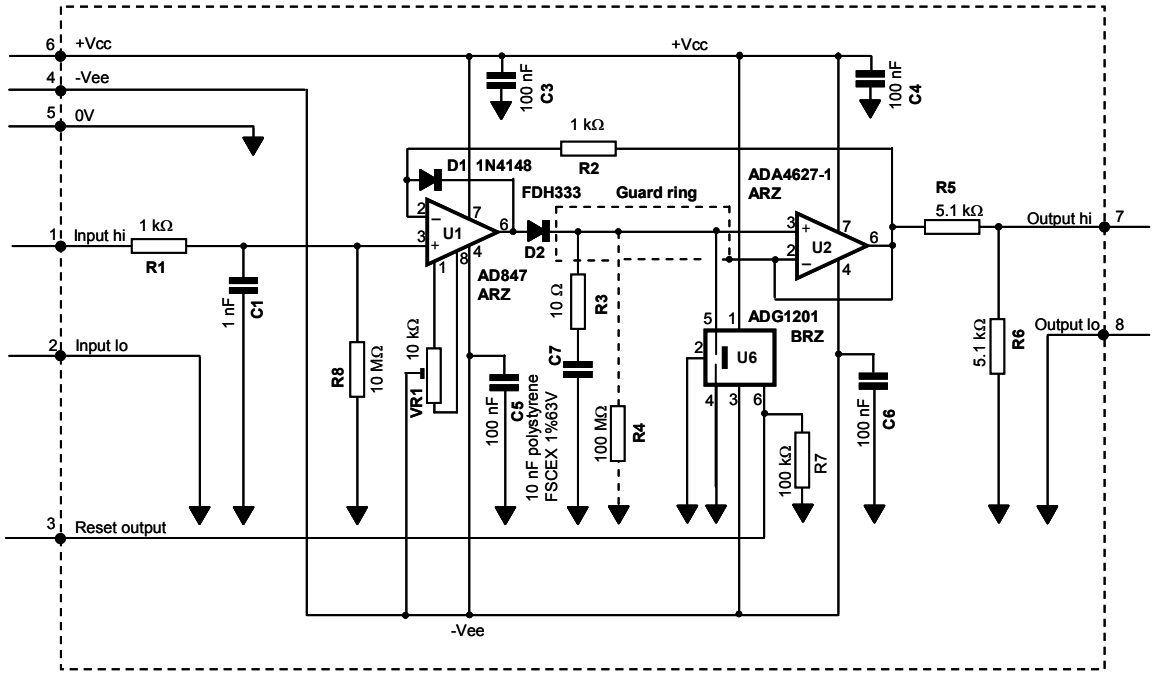

Figure 3: The basic peak detector circuit, version A.

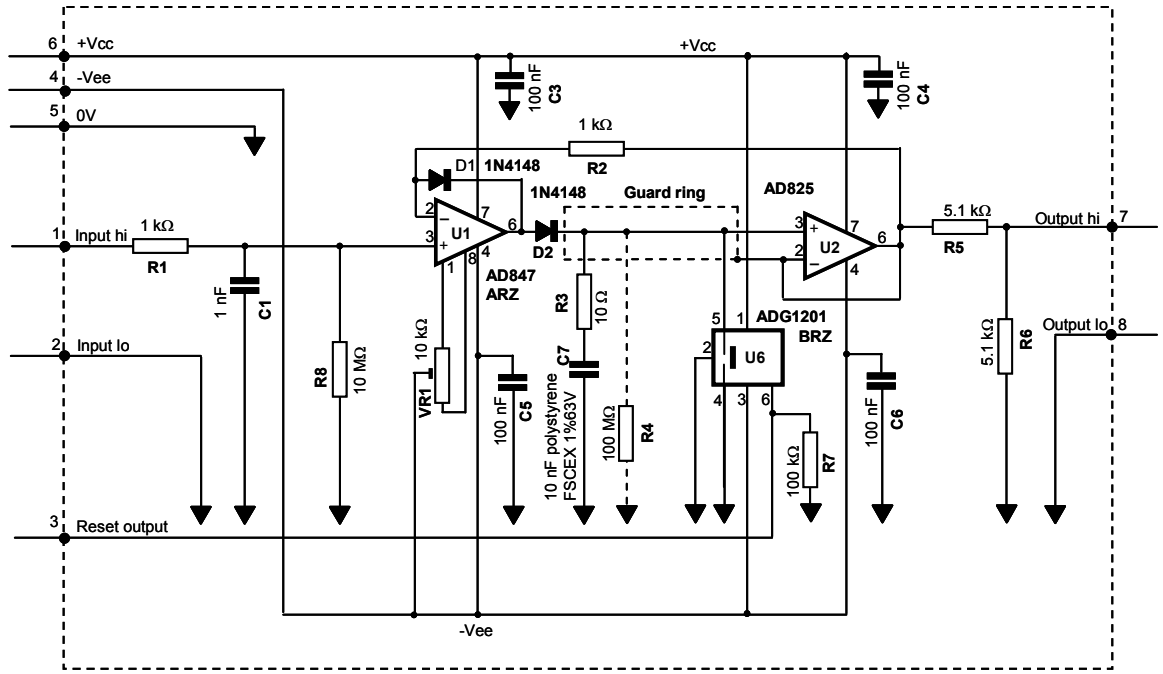

Figure 4: The basic peak detector circuit, version B.

The peak detector versions shown in Figures 5 and 6 are essentially similar to those of Figures 3 and 4 but an input clamp has been added ahead of peak detector. A second ADG1201 analogue switch maintains the input at zero when the peak detector is reset. Capacitor C2 is then charged through R1 to whatever non-zero baseline voltage is present. The underlying assumption is that the duty cycle of the circuit is very low, with input events to be detected happening every few seconds or so. The value of C2 is adjusted appropriately to allow it to be charges by any previous electronics. Unfortunately you will have to do the sums here, and the underlying assumption is that anyone attempting to exploit the circuits presented here will be expert enough to do this.

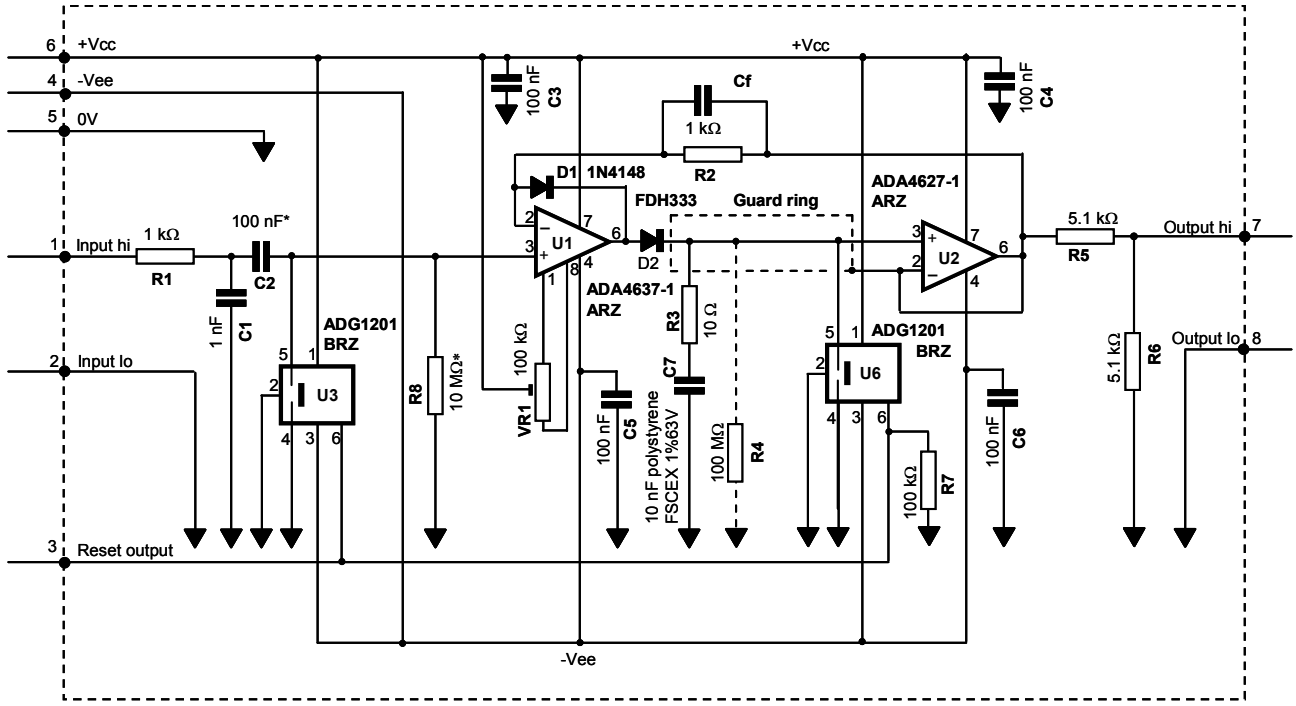

Figure 5: Circuit of peak detector circuit with input clamp. Version C. Capacitor Cf, empirically determined to be 150 pF, was soldered across R2; helps tame this particular opamp combination.

It is pointed out that the active and passive devices used in these circuits are not cast in stone. Rather it is intended that the reader will modify these appropriately for the application. Most SOIC amplifiers can be used but some combinations may result in output overshoot. Capacitor Cf, also shown on these circuits (in parallel with R2) can then be used to tame the response.

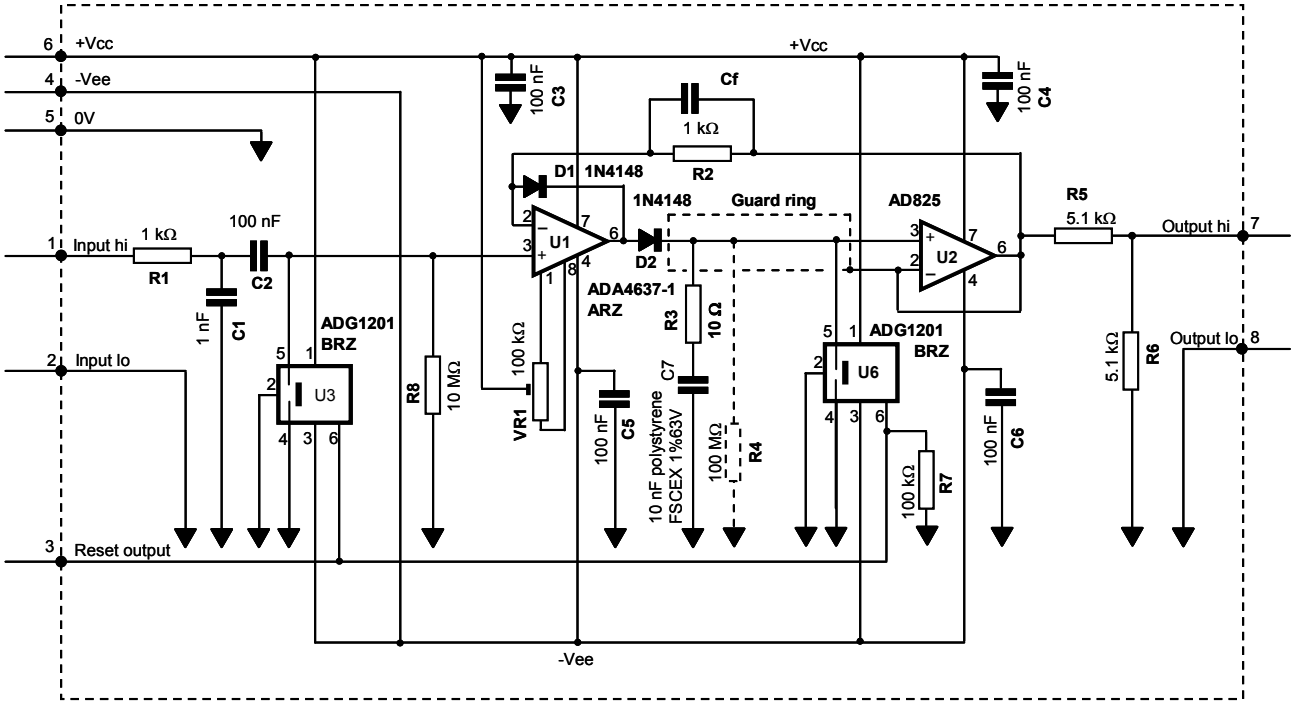

Figure 6: Circuit of peak detector circuit with input clamp. Version D. Capacitor Cf, empirically determined to be 150 pF, was soldered across R2; helps tame this particular chip combination.

For best performance ±12V or ±15V supplies should be used although lower voltages are acceptable, particularly for the negative supply, here the use of a -5V supply is perfectly adequate. Current consumption depends on opamps and the load used, and not significantly high. It is,

however, recommended that larger value supply decoupling capacitors are used off-board. Indeed, in our test set-up, shown in Figure 7, we did exactly this. Oscilloscope probes are all well and good, but BNCs are sometimes more convenient!

It is likely that using a pair of OPA365 amplifiers would result in a significantly improved performance, provided a higher speed charging diode used, and particularly if a lower forward voltage Shottky diode is used. In that case, the power supplies should be reduced to -200 mV negative and to +5V positive. This inevitably restricts the maximum output to just under 5V and it is left to the reader to decide whether this will be adequate for their application.

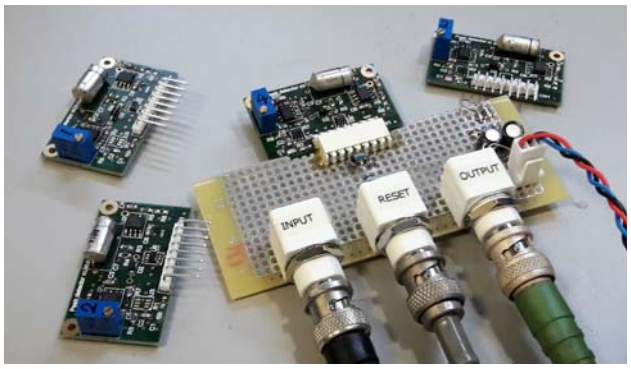

Figure 7: Arrangement used to test the peak detectors. Two 10 µF electrolytics decouple the power rails while a 470 Ω resistor and a small Zener protect the reset input from overzealous pulse generator settings.

The 'hold' or droop performance of the circuits described here is largely determined by the leakage performance of the charging diode.

Very low leakage diodes are hard to find these days. Siliconix did produce the PAD series pA leakage diodes a while back. Variants are still available form Linear Systems[14], though a home-brew low leakage diode can be readily made from a JFET, as described an old Burr-Brown application note[15], using for example an MMBF4117 JFET (drain and source wired together). Other low leakage diodes include the BAS416 or the FJH1100 or the FJH1101. Hardier experimenters will use bipolar transistors wired to act as diodes. A good old bipolar like the 2N3904 will exhibit <1 pA of reverse leakage when using its base-emitter junction. However, it morphs into a zener diode at just over 6.5 V. Clearly this approach is excellent when working with signal amplitudes below 5V. Higher reverse voltage at the expense of higher leakage current and is achieved by making the base the anode and the collector the cathode. Now the leakage current will be typically around 10 pA and a higher forward current can be supported. Remember though that the resulting diode will not be a high speed one. If high speed is required, then the collector must be shorted to the base and now we will be back at square one: the reverse voltage must be limited to <5V. As so often happens, the proverb 'horses for courses' comes into play.

5. Construction

The circuit is constructed on a small printed circuit board, 43x25 mm fitted with a right angle Molex KK series 0.1" pitch connector. Of course straight-through pins can also be used if required. All components other than D2 and C7 are of surface-mount type. The leaded components are used to allow different diodes and storage capacitors to be used. Surface mount polyester capacitors tend to have a large and variable surface area, so a through-hole arrangement was found to be more flexible.

The board design was developed with EasyPC[16] design software and constructed using hand soldering…OK provided you have either good eyesight, a good magnifier or both; but, hey, the components are pretty large really and the board is hardly a crowded one.

The design is shown in Figure 8, along with a constructed board. A ground plane is used on the bottom layer of the board, except below the inverting inputs of amplifier U1: additional capacitance there is never a good idea. Guard rings are provided around the charge hold capacitor…they would

[14] http://www.linearsystems.com/product.html
[15] Diode connected FET protects opamps application note, now available from Texas: http://www.ti.com/lit/an/sboa058/sboa058.pdf
[16] https://www.numberone.com/

come into their own when using low leakage diodes. A solder-link is provided close to the wiper of the input zero trimpot to cater for different opamp types, as noted in the circuits in Figures 3-6.

Printed circuit boards are available on request for a nominal charge.

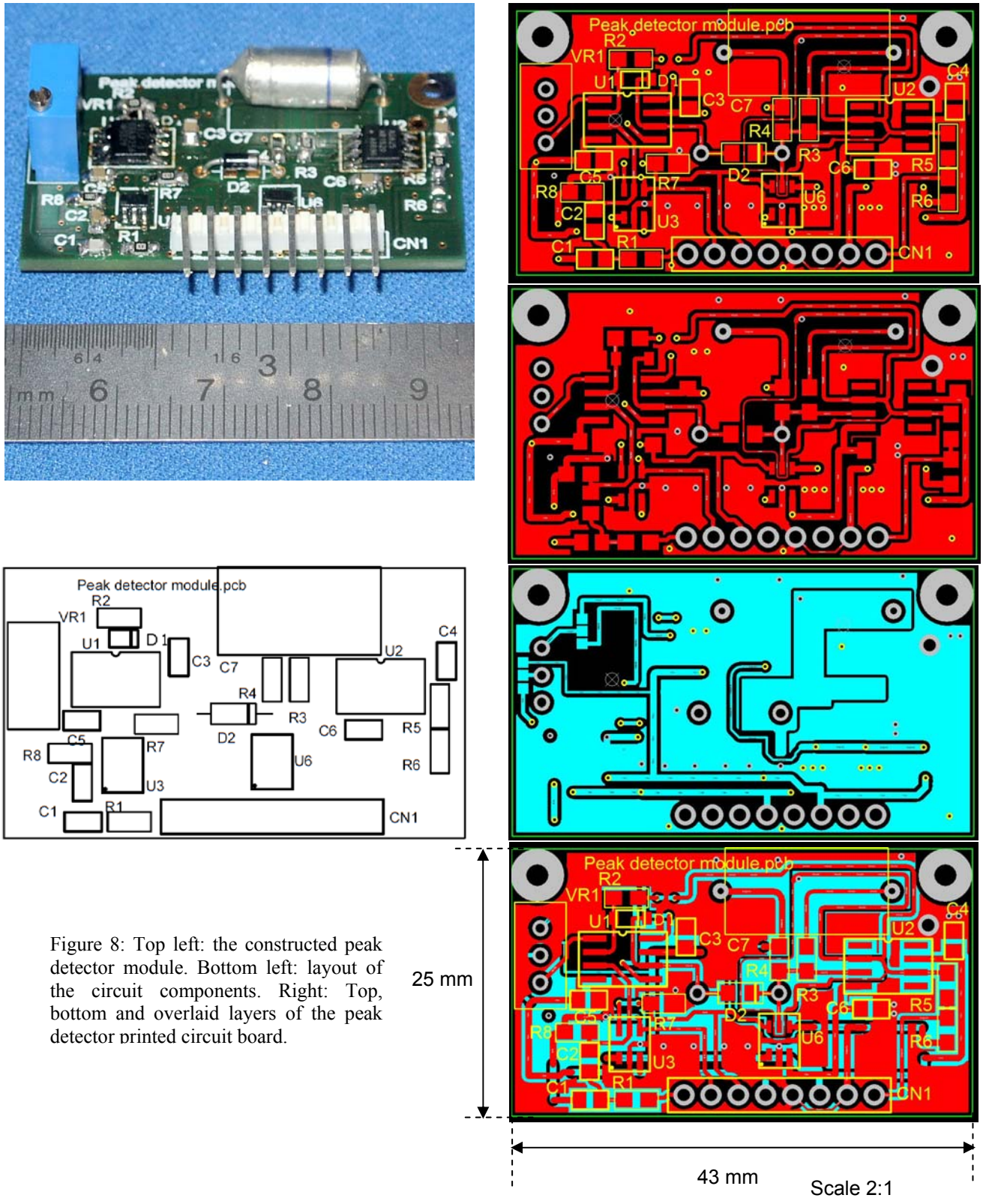

Figure 8: Top left: the constructed peak detector module. Bottom left: layout of the circuit components. Right: Top, bottom and overlaid layers of the peak detector printed circuit board.

6. How have others implemented peak detectors?

A similar circuit to that discussed here is presented by Ahrens[17] using now obsolete operational amplifiers. Costin and Opris[18] also presented a similar approach to that described here but implemented with discrete components. More recently, Presti *et al*[19] devised an approach where sequential peak detectors are used to improve linearity. An elegant solution has been presented by Haas and Dullenkopf in 1986[20] presented a similar solution to that presented here but employing a transconductance amplifier implemented in a hybrid circuit, with impressive performance and aimed at detecting narrow pulses and includes a peak event detection circuit. Transconductance amplifiers are indeed useful in peak detector circuits, taming the potential input amplifier overshoot but in practice it is not that straightforward. Of course one can make such amplifiers from discrete components (a better approach, though not so economic these days) or use the commonly available LM13700 device[21] that has limited bandwidth or use the much faster OPA615[22]….which also has a high input leakage current.

Meyer[23] presented a balanced detector circuit to eliminate the consequences of diode offset; this arrangement was primarily aimed at RF signal detection. Similarly a Linear Design Note[24] explored ways of balancing out diode offset using open-loop techniques. Kruikamp[25] and Chang[26] described peak detectors using CMOS techniques aimed at monolithic chip implementation of peak detectors, the former also using a transconductance amplifier.

An approach similar to our design but using two peak detectors in series (the first one of which was of relatively poor design) was described by Vetrivel and Sivaram[27], with the aim of increasing response speed. A superior, though complex design was presented by Buckens and Veatch[28]. This design has excellent dynamic range and linearity and was developed using numerous discrete components. I guess if you have NIM-bin[29], that's fine.

Approaches using comparators in the first amplifier stages have also been published[30], [31] and such approaches can be very fast indeed[32]. Interested readers are pointed to a Texas Instruments Application note[33] for a review of comparator performance. A somewhat different approach has been used in a Maxim application note[34] that uses a digipot as the storage element; his approach has

17 Ahrens T.I. (1998) An Improved Peak Detector. *Intersil Application note AN1097.*

18 Costin, D. Opris, P.(1995) High Speed Peak Detector For Glitch catching Used In Digital Storage Scopes", *IEEE*, 1995 DOI: 10.1109/SMICND.1995.494905.

19 Presti, C.D., Carrara, F., Scuderi, A., and Palmisano, G. (2007) Fast Peak Detector with Improved Accuracy and Linearity for High-Frequency Waveform Processing. *2007 IEEE International Symposium on Circuits and Systems.* DOI: 10.1109/ISCAS.2007.377887.

20 Haas, W. and Dullenkopf, P. (1986) A Novel Peak Amplitude and Time Detector for Narrow Pulse Signals *IEEE Transactions on Instrumentation and Measurement*, **IM-35**, No.4.

21 http://www.ti.com/product/LM13700 (the NE5517 by ON Semi (ex Philips) is similar)

22 http://www.ti.com/product/OPA615

23 Meyer, R.G. (1995) Low-Power Monolithic RF Peak Detector Analysis. *IEEE Journal Of Solid-State Circuits*, **30**, No 1.

24 Wright, J. (1992) Peak Detectors Gain in Speed and Performance. Linear Design Note DN-61. Uses open loop approach and diode biasing techniques.

25 Kruikamp M. W. and Leenaerts, D. M. (1994) A CMOS Peak Detect Sample and Hold Circuit, *IEEE Transactions on Nuclear Science*, **41**(1), pp 295-298.

26 Chang, P.Y. and Chou, H.P. (2006) A High Precision Peak Detect Sample and Hold Circuit. *IEEE Nuclear Science Symposium Conference Record* DOI: 10.1109/NSSMIC.2006.356168.

27 Vetrivel, L. and Sivaram, B. M. (1995) Computer-controlled high-speed peak detector for use with pulsed lasers. *Review of Scientific Instruments* **66**, 2394 https://doi.org/10.1063/1.1145636.

28 Buckens, P.F. and Veatch M.S. (1992) A High Performance Peak-Detect and Hold Circuit for Pulse Height Analysis, *IEEE Transactions On Nuclear Science,* **39**, No. 4.

29 https://en.wikipedia.org/wiki/Nuclear_Instrumentation_Module.

30 McLucas J. (2004) Precision peak detector uses no precision components. *EDN.*

31 Krehlik P. (2002) High-speed peak detector uses ECL comparator. *EDN.*

32 Jong-Hoon Kim, J.H., Shin, J.-B. Sim, J.-Y. and Park, H-J. (2011) 5-Gb/s Peak Detector Using a Current Comparator and a Three-State Charge Pump. *IEEE Transactions on circuits and systems II: Express Briefs*, **58**, 5, DOI: 10.1109/TCSII.2011.2124830.

33 Comparing the High Speed Comparators - Texas Instruments application note AN-87.

34 Inexpensive Peak Detector Features Droopless Operation. Maxim Application note 1163.

also been featured in a U-tube video[35]. A U-tube video on peak detectors, whatever next! This is a great approach when only an 8 bit resolution is acceptable and though higher resolution digipots are available, but there are none with a counter input. This approach was reminiscent of an approach used by the authors many moons ago when the Burr-Brown ADC700 analogue-to-digital converter was available. This wonderful 16-bit resolution chip featured successive-approximation architecture but uniquely provided access to both comparator inputs: Its internal digital-to-analogue converter output was accessible and could be fed to an external comparator that controlled the acquisition (i.e. sampling cycle). A real pity this device is no longer available but then it was in a hermetic 28-pin side-braze ceramic DIP package – cost – what cost! But the damn thing could sample in some 20 µs and provide a digital output at the same time. Nostalgia definitely is not what it used to be.

Interested readers will no doubt also wish to visit other sites[36, 37, 38].

7. Performance

The testing was performed in conjunction with the jig shown in Figure 7. The signal source was a Metrix GX320 function generator, the reset pulse generator was a Global Specialities Corporation 4001 (a long discontinued device, that still provides us with excellent performance even after 25+ years of use (!) and for monitoring we used a Tektronix TDS 2024C 'scope and a Fluke 115 multimeter. The output resistors were out of circuit to provide a unity input-output gain (almost, there is a slight (~0.01%) attenuation at the input due to R1 and R8.

Starting with large signals, 20 V peak-peak input, i.e. 10 V peak, all versions of the basic circuit respond well and settle correctly, but there is a hint of something going wrong with the circuits that use the FDH333 so-called low leakage charging diode: the output drops slightly during the negative input half cycles. The bog standard 1N4148 diode does well though.

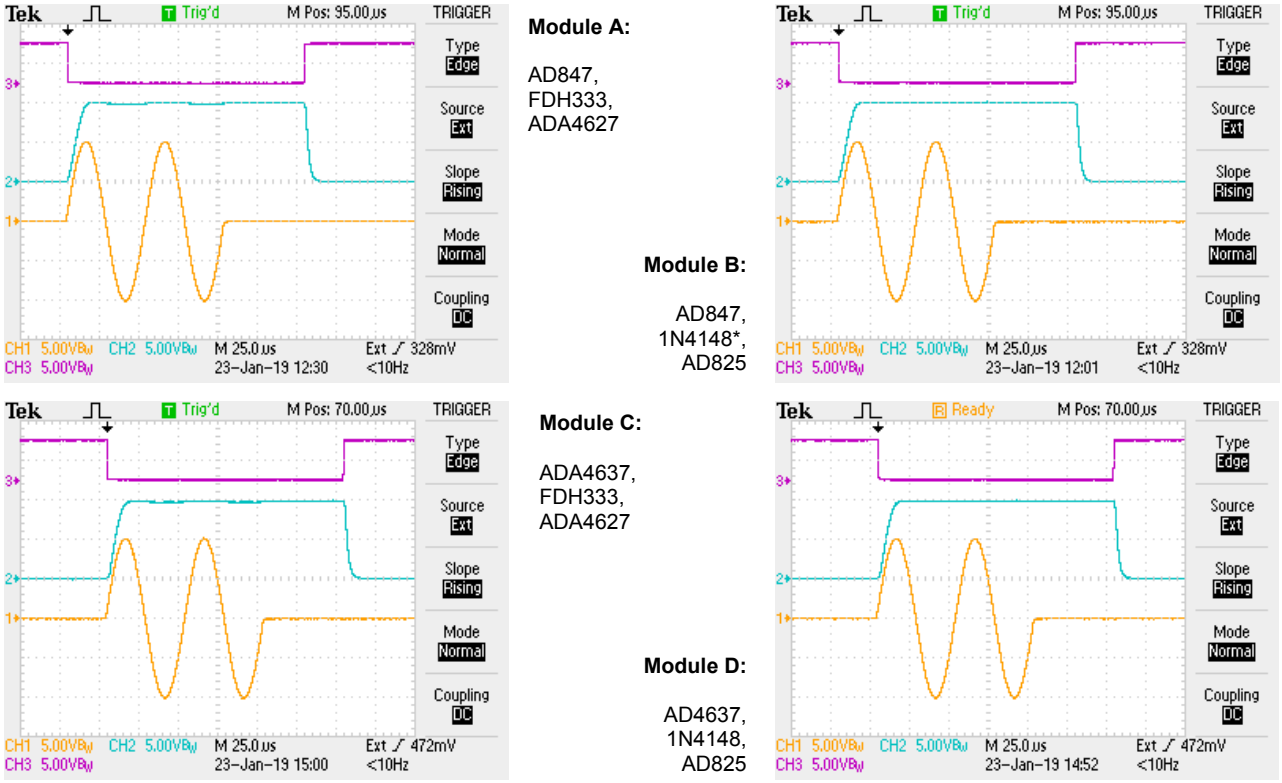

Figure 9: Response of the four versions of the circuit to 20 V peak-peak two cycle sine burst at 20 kHz. The reset signal (pink) takes the circuit out of reset just before the input burst (yellow); output is the blue trace (* = SM).

35 http://www.analogzoo.com/2016/02/a-100khz-zero-droop-peak-detector/
36 https://ieeexplore.ieee.org/iel5/101/4099335/04099508.pdf
37 http://sound.whsites.net/appnotes/an014.htm.
38 https://www.sciencedirect.com/topics/engineering/peak-detector.

When the input amplitude is reduced 10-fold to 2 V peak-peak, all versions perform admirably, as shown in Figure 10.

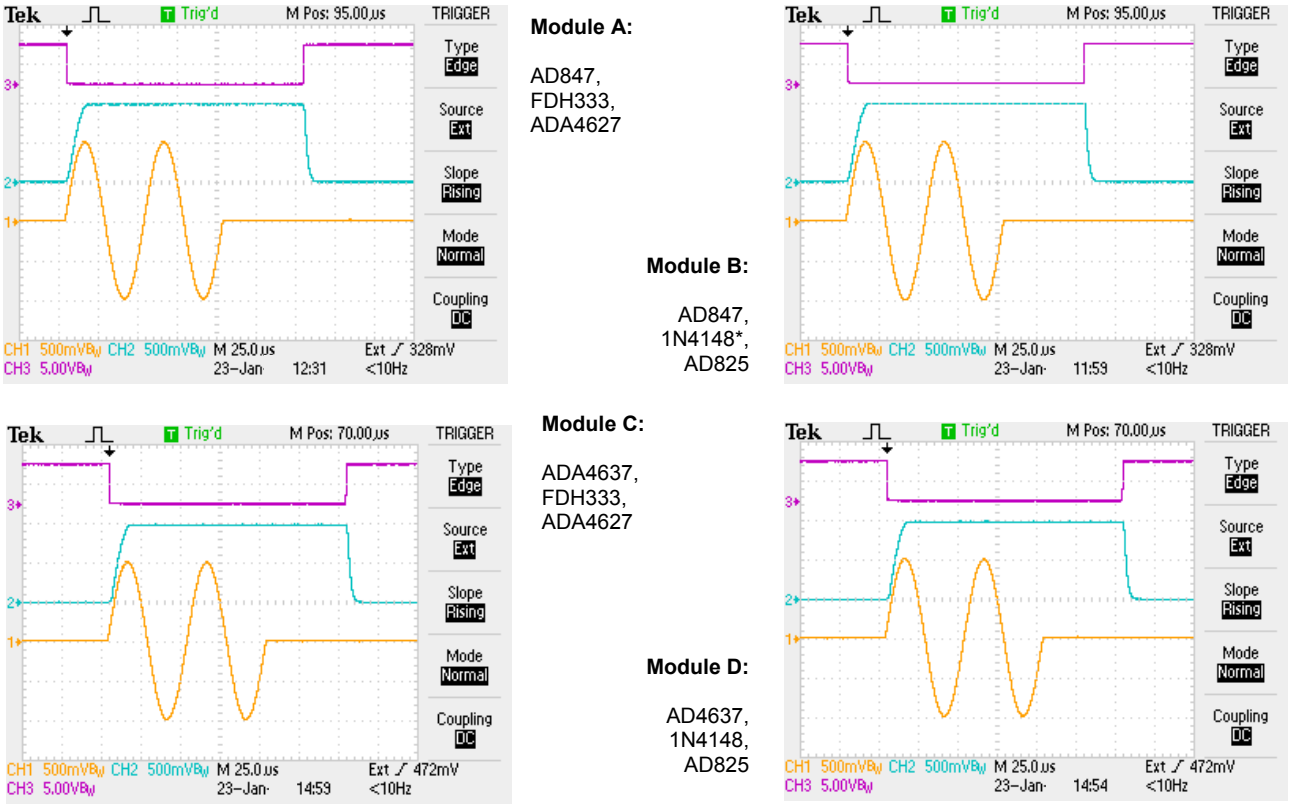

Figure 10: Response of the four versions of the circuit to 2 V peak-peak two cycle sine burst at 20 kHz. Trace colours as in Figure 9.

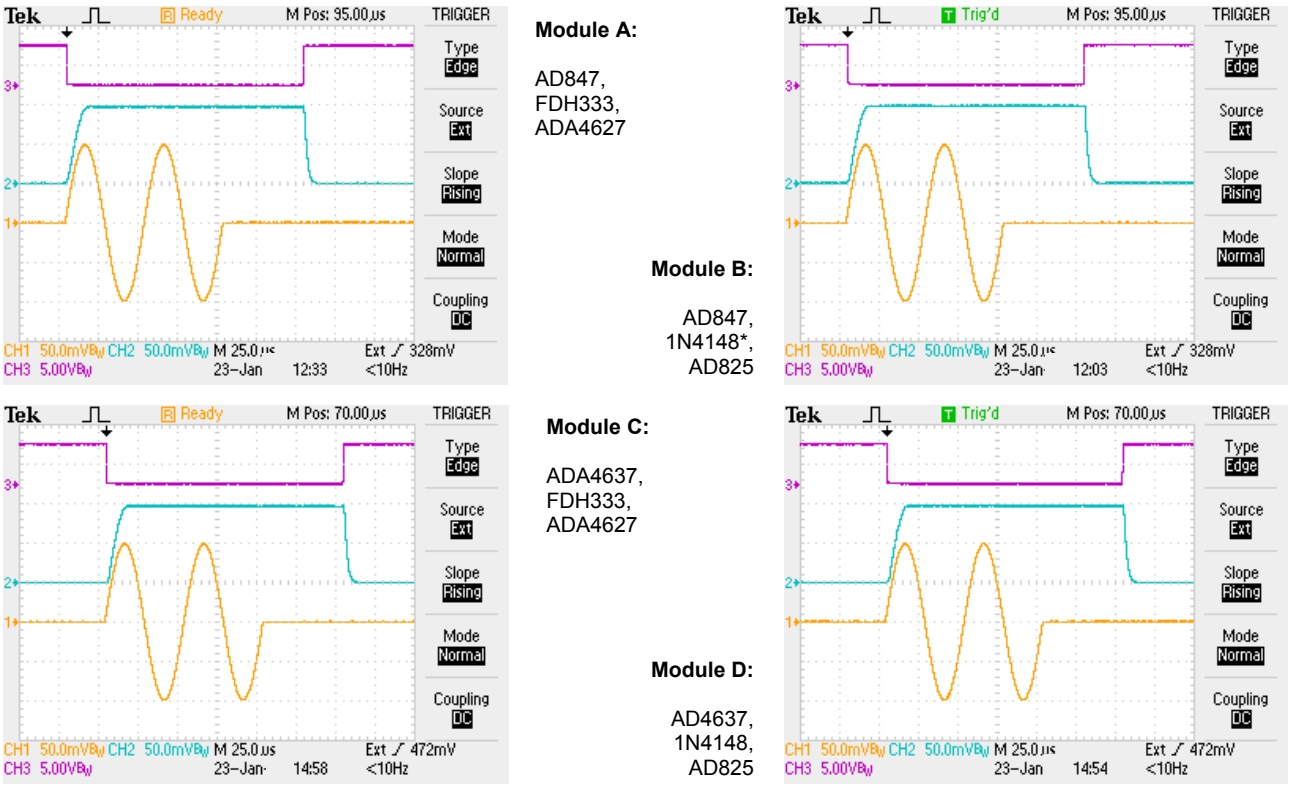

Figure 11: Response of the four versions of the circuit to 200 mV peak-peak two cycle sine burst at 20 kHz (* = surface mount).

Further reduction to 200 mV peak-peak input also provides perfectly adequate outputs for all versions, as shown in Figure 11. The responses of the modules to further reduction of input signal, down to 10 mV peak input seem to now indicate differences, as shown in Figure 12. Firstly, Version B seems to exhibit some slight charge feedthrough from the reset line, presumably form the higher loop bandwidth band width associated with the combination of the AD847 and the AD825. Secondly, the outputs do not seem to settle to the correct value of 10 mV. A couple of things come into play here (1) no attempt had been made at that point to correct for the input offset variations of the various input operational amplifiers; the AD847's input offset specification is somewhat worse than that of the ADA4637 and (2) there is no guarantee that the generator output voltage is zero. The later in fact is somewhat troublesome as the generator's offset adjustment is quite coarse, in steps of 1 mV. We managed to measure it by various approaches and estimated to be ~ -0.7 mV.

Too much should thus not be read in the apparent performance depicted in Figure 12. We just did not have the required test equipment to properly evaluate the circuit performance. Rather, the take-home message is that all versions perform surprisingly well at this low input voltage and any of the variants would be quite acceptable provided appropriate offset adjustment is carried out.

We note that the clamping circuits were not active during the acquisition of these measurements (a short was applied across C2).

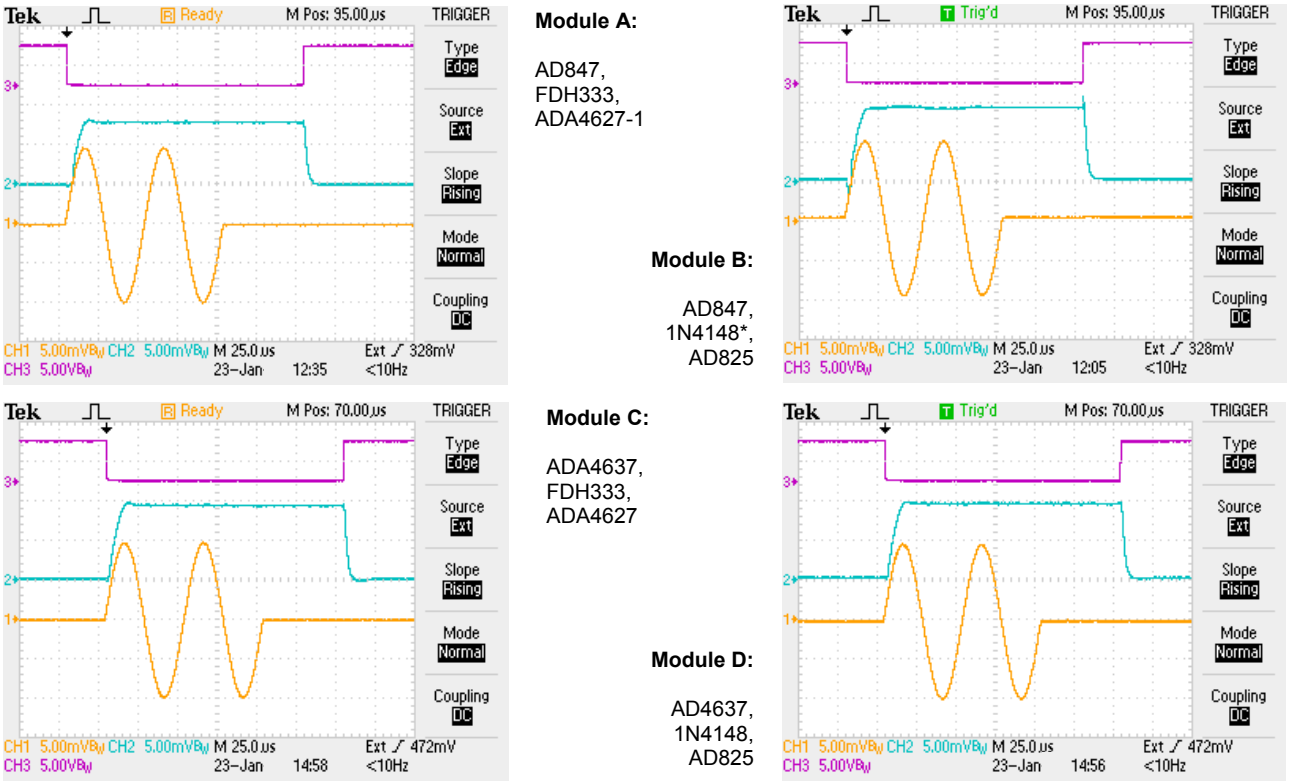

Figure 12: Response of the four versions of the circuit to 20 mV peak-peak two cycle sine burst at 20 kHz (* = surface mount).

What about the hold or droop performance? Well, we have to admit to a bit of embarrassment here. All the data shown in Figure 13 were obtained with a shunt resistor, R4, 100 MΩ, across the holding capacitor; trouble is, we forgot that it was in circuit when we acquired the data; senility, ah, senility.

The 10 nF/100 MΩ time constant is 1 second. Starting with a peak detector output voltage V of 1 V, we would expect the output voltage, after 500 ms, $V_{0.5sec}$, to be:

$$V_{0.5sec} = 1 \times e^{-0.5} = 2.71828^{-0.5} = 0.607 \text{ V}.$$

What do we get for all modules except Module B? Just over 0.4 V…so that kinda fits. Module B seems to have a shunt resistance of ~50 MΩ. Did we solder the wrong resistor in? Was there some flux left across contacts? Either of any of those is likely, probably. The only proper way of figuring out what is going is to measure the droop response without the resistor in place.

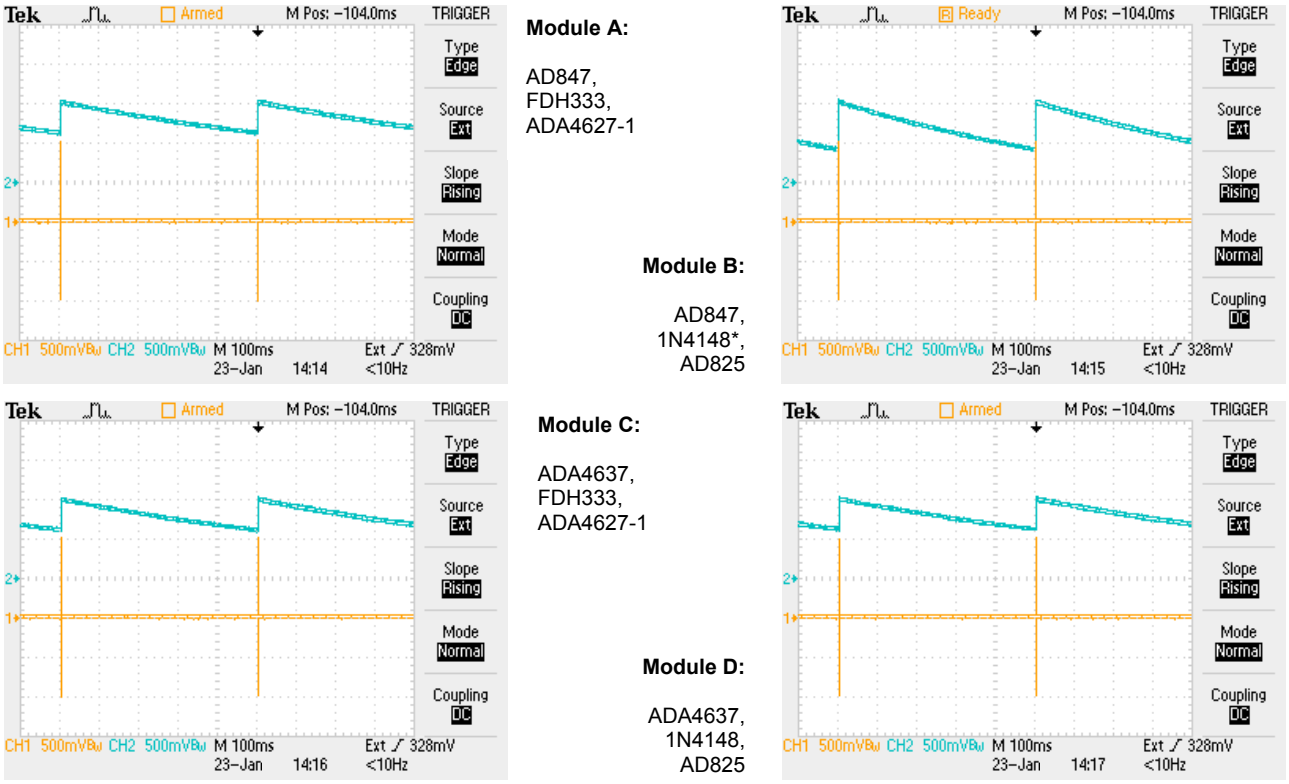

Figure 13: Droop performance of the circuit versions following sine monocycles at 2 Hz; discharge resistor R4 in place (* = surface mount).

The data obtained without R4 in place are shown in Figure 14. We see that the droop rate associated with Modules A, C, D is <10 mVsec^{-1}. Using the well-known relation:

$$i \times t = C \times V,$$

the leakage current can be determined to be = 10^{-8} F x 10 x 10^{-3} V/ 1 sec = 10^{-10} A or 100 pA. That is a reasonable figure since the input leakage currents of all the operational amplifiers used for U2 are specified to be less than 10 pA and the ADG1201 switch contributes <4 pA. The diode reverse leakage current of course contributes to the leakage rate, but here things get awkward. For the FDH333 the leakage is specified at 1 nA…but with a reverse voltage of 125 V, so not quite the operational conditions shown in Figure 14. With just a few volts of reverse bias, the leakage current is much, much reduced. A similar story applies to the popular 1N4148, specified to be <25 nA maximum@20V, with no typical values specified, but the actual values vary from manufacturer to manufacturer. In practice we found in numerous other projects that the 1N4148 performs very well indeed. All this applies at room temperature; at high temperatures the leakage current inevitably increases and this should be taken into account if operation at higher temperatures is envisaged.

Module B performs very badly indeed. In that particular module, we used a surface-mount version of the 1N4148, a 1N4148W-13-F. This is specified with a leakage current of 1 µA maximum! It seems to have a leakage of 50 nA at room temperature. We should have used a 1N4148WSQ-7-F, which has similar specifications as the glass 1N4148. Better still would be to use a BAS416, properly specified for low leakage work (3 pA typical, 3 nA at high temperature). The take-home message is to read data sheets carefully and to experiment, taking note that long hold times should be avoided if at all possible; something has to give (increase hold value capacitor and accept poorer

high frequency performance) if these are considered essential. In practice, the peak detector output should be digitised as soon as possible following the transient event; a value a few milliseconds should be aimed for.

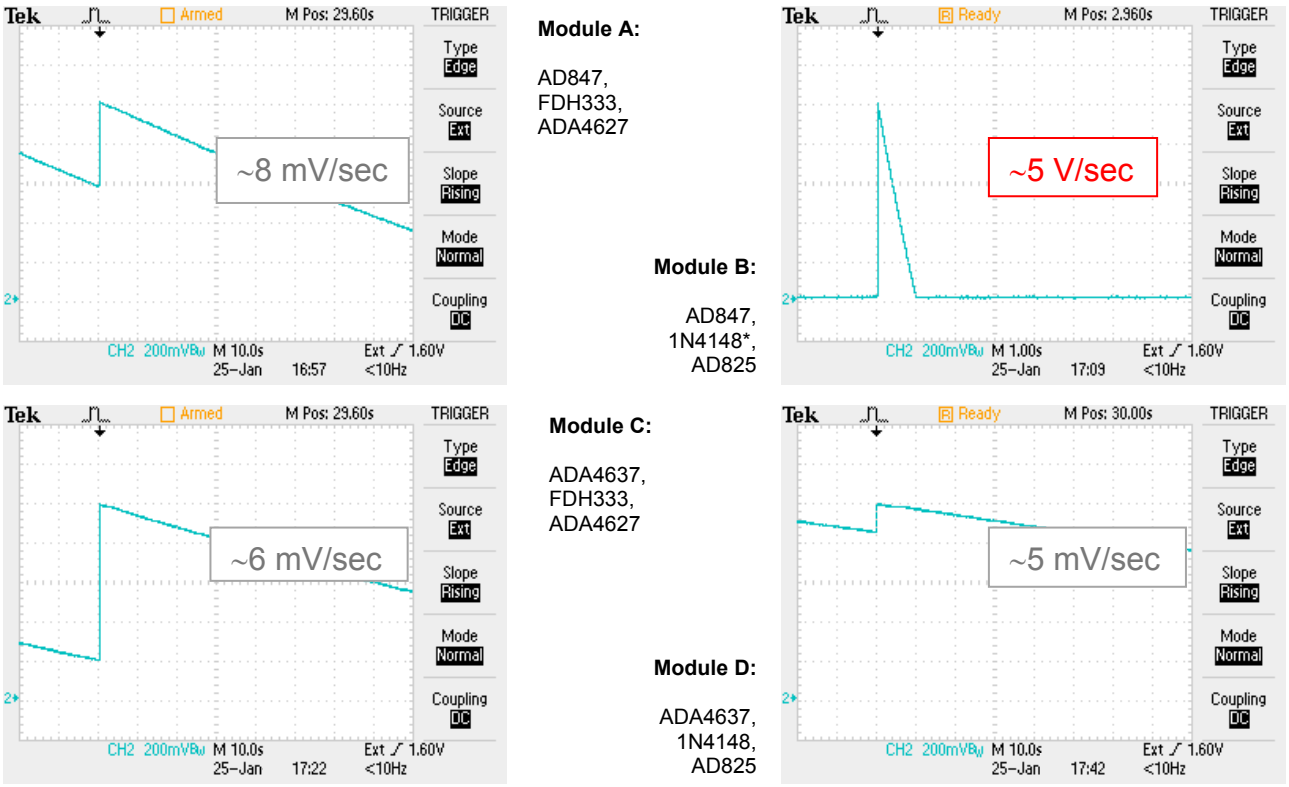

Figure 14: Droop performance of the circuit versions following single sine monocycles; discharge resistor R4 not fitted. The single cycle input trace (2 V peak-to-peak) is not shown since it could not be viewed anyway at these long timebase settings. Note the position of the channel 2 ground cursor! It is only the slope that is critical here and we made no attempt to 'fire' the input at any specific time, hence the difference in shapes of the traces; we just waited for about 1 minute before the previous trigger before enabling single-shot 'scope operation. (* = surface mount)

A really clean board is required to achieve the low leakages reported here. After the components are soldered in place it is recommended that a good solvent cleaner is used to remove all traces of solder flux, particularly around the printed circuit board guard ring. There are some pretty thin tracks there …surface mount components do have some disadvantages! The purists may wish to use the air-mount approaches, soldering all the critical high impedance hold components in mid-air as in the good old days. Note that any leakage paths around the diode will also compromise performance, but <10 $mVsec^{-1}$ should be achievable.

A second crucial aspect of performance is linearity. Here further nightmares can easily take place. Large outputs are no problem, but when attempting to determine performance at millivolt input levels, difficulties are inevitable. Unfortunately very few signal generators have negligible DC output levels; the more versatile the generator the worse the output offset and the less can it be adjusted to true zero. To some extent this can be taken care of with the on-board offset control but 'truth' is hard to get to. This can be seen in Figure 15 which shows the output voltage as a function of input voltage. Below about 50 mV or so, the input offset trimmer should be adjusted correctly (traces A, D); when no adjustment is made (traces B, C) the performance seems worse, but actually reflects the generator output offset. Measurements with a calibrated input attenuator indicate that the linearity of the system(s) is well within ±0.2 dB and can be improved to be within ±0.1 dB from 2 mV to 10 V, well within ±1%.

A third aspect of performance tested was the frequency response of the different arrangements. This is shown in Figure 16. Once again, we see that some limitations of the test instrumentation play a role.

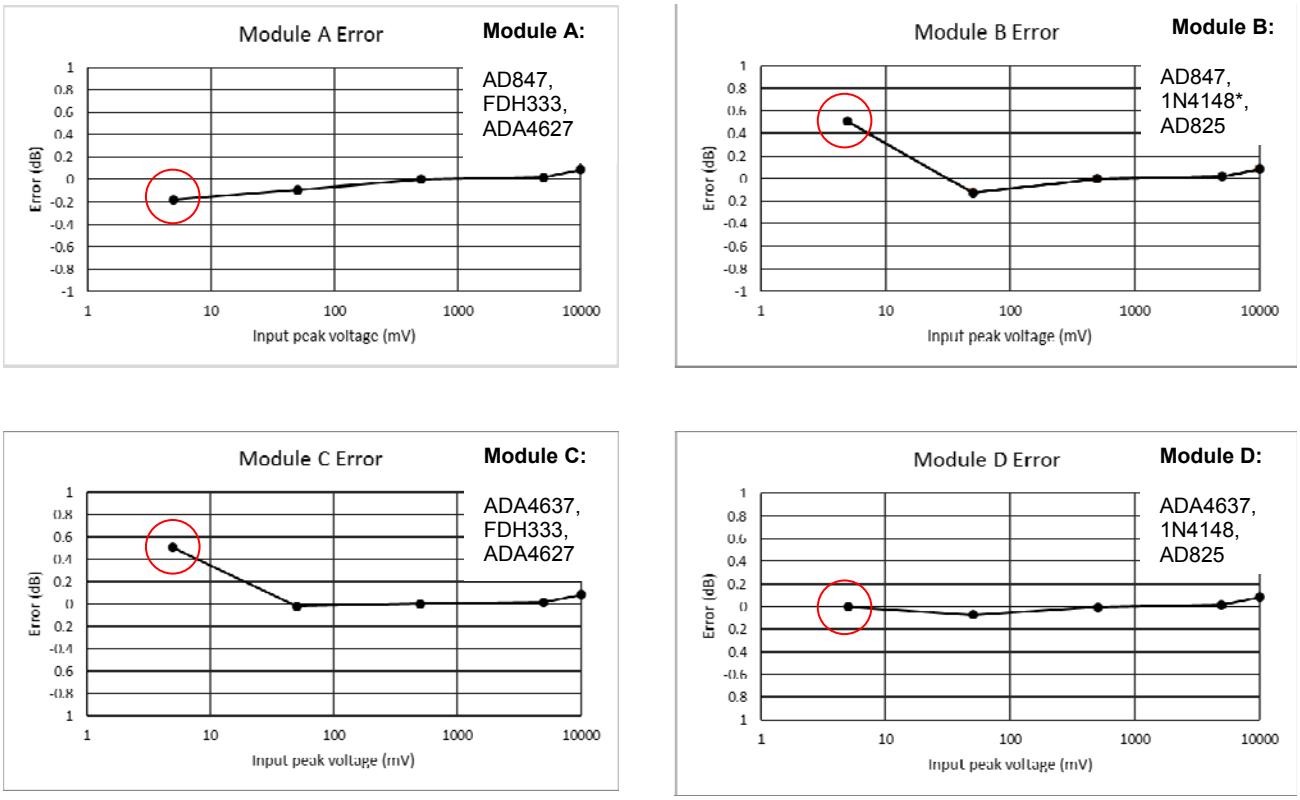

Figure 15: Amplitude response of the four versions of the circuit using a continuous 5 kHz sinewave input. The circled readings should be taken with a large pinch of salt and depend on input offset adjustment; see text for explanations.

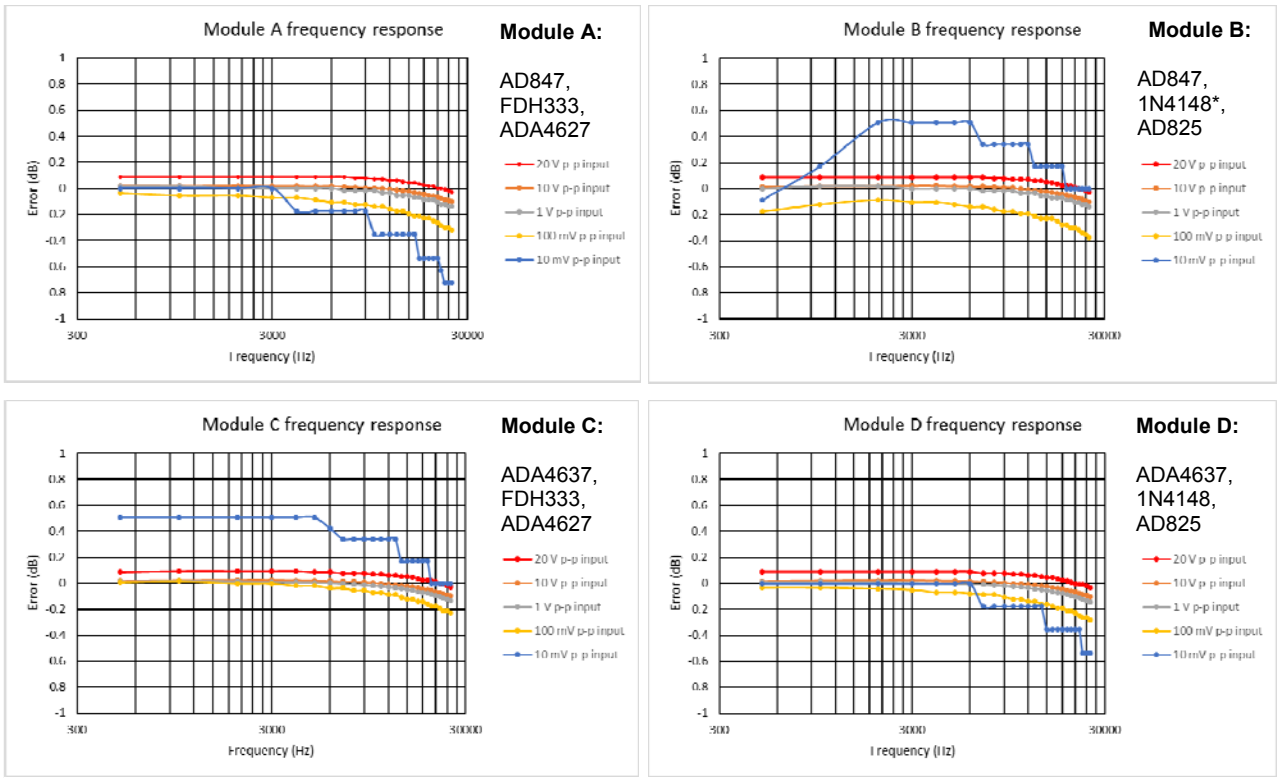

Figure 16: Frequency/amplitude response of the four versions of the circuit at different input levels (continuous sine wave input); (* = surface mount).

There is a consistent increase in output of ~0.1 dB at the highest amplitude setting (20 V peak-to-peak) due to the combined effects of the generator and digital voltmeter used. The effects of incorrect input offset adjustment and output indicator are even more obvious here: the blue traces are clearly quantised as our output meter resolution was 0.1 mV and the absolute error depends on the offset setting. The frequency response is just as expected: at low frequencies all is well, but at 10 kHz and above the output is progressively lower at lower input amplitudes. The charging amplifier U1 has to work harder and harder to overcome the charging diode offset voltage. This is where 'specmanship' comes in! If we ignore the error of the 'red' traces (20 V peak-to-peak), we can say that the output is well within -0.7 dB at up to 20 kHz at all input voltages above 5 mV. This is pretty respectable for a simple circuit. A reduction of the charging capacitor improves the frequency response as would be expected (data not shown) but the droop rate obviously increases. Moreover, it does not matter too much which pair of operational amplifiers is used, again, not too much of a surprise as they are all wide bandwidth devices.

What about the input clamp? The performance of module C and D, the only ones fitted with a clamp circuit, is shown in Figure 17. The input clamp does just it is supposed to do: whatever input voltage is present when the 'reset' signal is deactivated is assumed to be zero and only subsequent peaks are held. The astute reader will note that a bit of a circular argument is used here. We say that

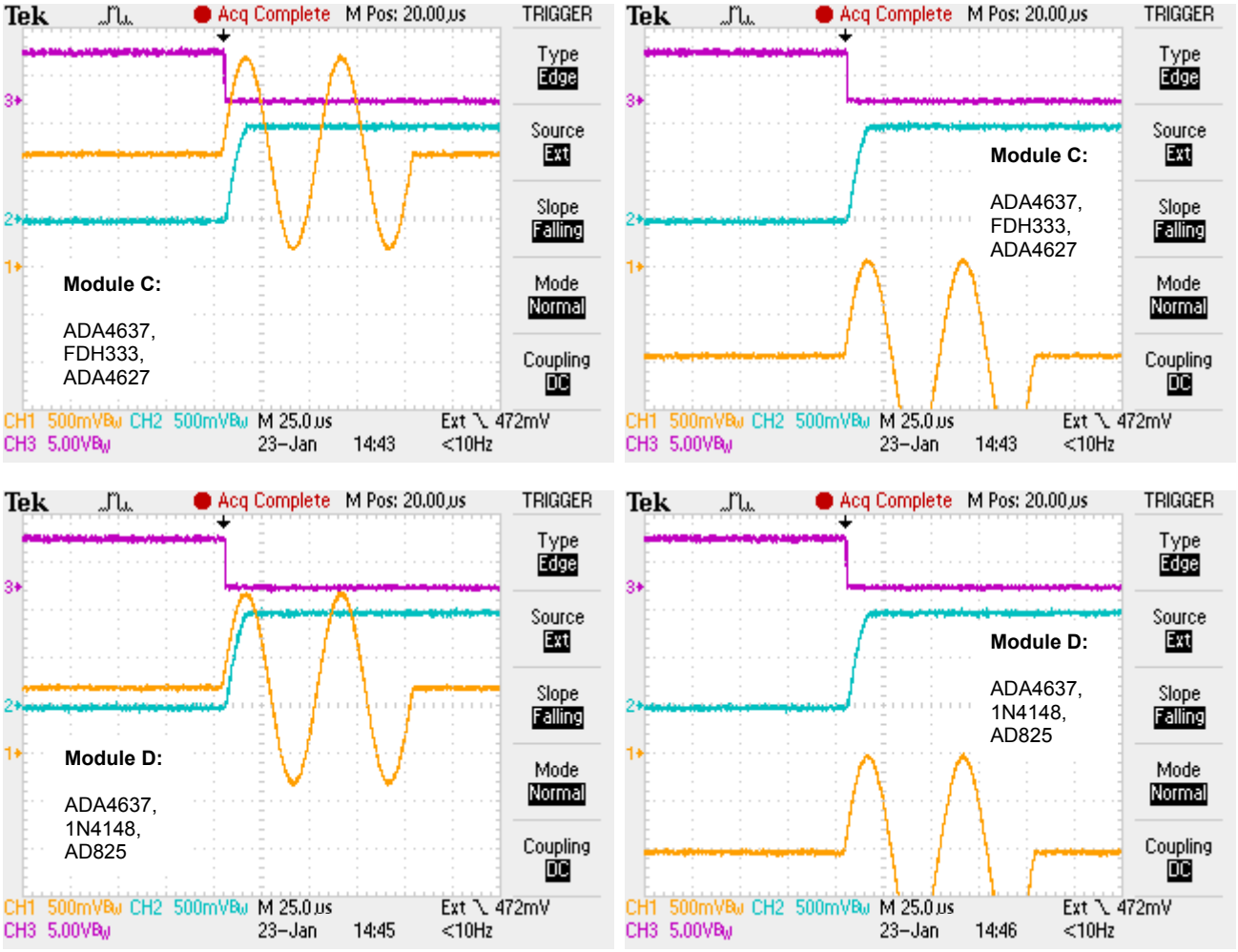

Figure 17: Performance of the clamping circuits for modules C (top) and D (bottom). The clamp circuit performs equally well for both positive and negative DC input voltages.

we use a peak detector is used when we don't know when the signal will arrive – so when should the reset be disabled? The data shown in Figure 17 can thus be considered to be a fudge. In reality it is not that bad: we should know, usually at least (!), the approximate time when we expect the

signal and can take the reset line low. If we take it low much too early, whatever charge is stored on capacitor C2 will discharge through R8 (time constant 1 sec for values shown in circuits) but the values of these components can be altered to suit the application. In that respect, choosing an ADA4637 for the input amplifier is preferable as this is a FET input device, allowing us to increase R8's value to >100 MΩ, or even eliminating altogether if we are sure that the input will not exceed amplifier specifications. Typically the reset line can be taken low a few milliseconds before the expected event.

It is expected that capacitor C2 will spend most of its time charging, i.e. that the circuit will be mostly in a reset state. Dielectric absorption is thus unlikely to play a role here. However, the devices driving our circuit must be able to charge the capacitor quickly enough; in practice preceding circuits will consist of operational amplifiers and most can easily provide the required charging current. Remember that the clamping circuit is intended to take out small offset voltages and is not expected to be used at fast times. The reset line is thus expected to be high for 1 ms at least – this is not an ultra-fast clamp! The same goes for hold capacitor reset of course, the longer the better.

8. List of components

This becomes ever so slightly messy because we are dealing with four different versions of the circuit and we made a mistake in the chip numbering when we laid out the printed circuit board…what should have been U4 ended up being called U8. Well it didn't actually do that, it is one of us who made the mistake and B Vojnovic doesn't really 'do' pcbs and the reader is left to decide who made the mistake. All the electronic components are readily available and total cost is ~£35, potentially less if you shop around.

Version A

ID	Item	Description	Manufacturer	Model #	Supplier	Part #	Total
--	Printed circuit board Double-sided	Filename: Peak detector module.pcb	Gray	--	Beta Layout	---	9.11
CN1	DC power input header	8 way Molex 0.1" right angle	Molex	22-05-2081	OneCall	9731237	0.572
U1	Input operational amplifier,	50 MHz, 300 V/µs, ± 4.5V to ± 18V, SOIC-8	Analogue Devices	AD847ARZ	OneCall	2305605	5.99
U2	Output operational amplifier	19 MHz, 78 V/µs, ± 5V to ± 15V, SOIC-8	Analogue Devices	ADA4627-1ARZ	OneCall	1827378	6.63
U8	Reset analogue switch,	SPST, 1 channel, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
D1	Negative clamp diode	Small signal diode, single, 75 V, 150 mA, 1 V, 4 ns	Taiwan Semi	TS4148 RYG	OneCall	2708389	0.036
D2	Peak charging diode	Signal Diode, Single, 100 V, 150 mA, 1 V, 4 ns, 2 A	Multicomp	1N4148 (DO-35)	OneCall	2675146	0.0317
R1	Input low pass filter resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R2	Feedback resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R3	Charging limit resistor	10 Ω 1% 0805 125mW	Vishay	CRCW080510R0FKEA	OneCall	1469859	0.024
R4	Peak hold leak resistor	100 MΩ 1% 0805 125mW	Vishay	CRCW0805100MJPEAHR	OneCall	2395992	0.343
R5	Output series resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R6	Output shunt attenuator resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R7	Reset pull-down resistor	100 kΩ 1% 0805 125mW	Vishay	CRCW0805100KFKEA	OneCall	1469860	0.024
R8	Input pull-down resistor	10 MΩ 1% 0805 125mW	Vishay	CRCW080510M0FKEA	OneCall	1469858	0.028
VR1	Offset adjust trimpot	10 kΩ trimmer 12 turns, 3266 series, 250 mW, ± 10%	Bourns	3266W-1-103LF	OneCall	9352651	3.88
C1	Input low pass filter capacitor	1 nF 0805, 50V, 50 V, X7R	AVX	08055C102JAT2A	OneCall	1833879	0.148
C3	U1 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C4	U2 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C5	U1 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C6	U2 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C7	Peak hold capacitor	10 nF 63V - Polystyrene, 10000 pF, 63 V, ± 1%, FSC/EX Series	LCR Components	FSCEX 10000PF 1% 63V	OneCall	9520414	1.81
						TOTAL	**31.70**

Version B

ID	Item	Description	Manufacturer	Model #	Supplier	Part #	Total
--	Printed circuit board Double-sided	Filename: Peak detector module.pcb	Gray	--	Beta Layout	---	9.11
CN1	DC power input header	8 way Molex 0.1" right angle	Molex	22-05-2081	OneCall	9731237	0.572
U1	Input operational amplifier,	single, 50 MHz, 300 V/µs, ± 4.5V to ± 18V, SOIC-8	Analogue Devices	AD847ARZ	OneCall	2305605	5.99
U2	Output operational amplifier	single, , 41 MHz, 140 V/µs, ± 5V to ± 15V, SOIC-8	Analogue Devices	AD825ARZ	OneCall	9603735	4.07
U8	Reset analogue switch,	SPST, 1 channel, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
D1	Negative clamp diode	Small signal diode, single, 75 V, 150 mA, 1 V, 4 ns	Taiwan Semi	TS4148 RYG	OneCall	2708389	0.036
D2	Peak charging diode	Small signal diode, single, 75 V, 150 mA, 1 V, 4 ns	Taiwan Semi	TS4148 RYG	OneCall	2708389	0.036
R1	Input low pass filter resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R2	Feedback resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R3	Charging limit resistor	10 Ω 1% 0805 125mW	Vishay	CRCW080510R0FKEA	OneCall	1469859	0.024
R4	Peak hold leak resistor	100 MΩ 1% 0805 125mW	Vishay	CRCW0805100MJPEAHR	OneCall	2395992	0.343
R5	Output series resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R6	Output shunt attenuator resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R7	Reset pull-down resistor	100 kΩ 1% 0805 125mW	Vishay	CRCW0805100KFKEA	OneCall	1469860	0.024
R8	Input pull-down resistor	10 MΩ 1% 0805 125mW	Vishay	CRCW080510M0FKEA	OneCall	1469858	0.028
VR1	Offset adjust trimpot	10 kΩ trimmer12 turns, 3266 series, 250 mW, ± 10%	Bourns	3266W-1-103LF	OneCall	9352651	3.88
C1	Input low pass filter capacitor	1 nF 0805, 50V, 50 V, X7R	AVX	08055C102JAT2A	OneCall	1833879	0.148
C3	U1 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C4	U2 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C5	U1 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C6	U2 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C7	Peak hold capacitor	10 nF 63V - Polystyrene, 10000 pF, 63 V, ± 1%, FSC/EX Series	LCR Components	FSCEX 10000PF 1% 63V	OneCall	9520414	1.81
						TOTAL	**29.15**

Version C

ID	Item	Description	Manufacturer	Model #	Supplier	Part #	Total
--	Printed circuit board Double-sided	Filename: Peak detector module.pcb	Gray		Beta Layout	---	9.11
CN1	DC power input header	8 way Molex 0.1" right angle	Molex	22-05-2081	OneCall	9731237	0.572
U1	Input operational amplifier,	Single, 79.9 MHz, 170 V/µs, ± 5V to ± 15V, SOI- 8	Analogue Devices	ADA4637-1ARZ	OneCall	2067786	6.51
U2	Output operational amplifier	Single,19 MHz, 78 V/µs, ± 5V to ± 15V, SOIC-8	Analogue Devices	ADA4627-1ARZ	OneCall	1827378	6.63
U3	Clamp analogue switch	SPST, 1 channel, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
U8	Reset analogue switch	SPST, 1 channel, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
D1	Negative clamp diode	Small signal diode, single, 75 V, 150 mA, 1 V, 4 ns	Taiwan Semi	TS4148 RYG	OneCall	2708389	0.036
D2	Peak charging diode	Small signal diode, 150 V, 200 mA, 1.15 V, 1 A, low leakage	On Semiconductor	FDH333	OneCall	9843760	0.17
R1	Input low pass filter resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R2	Feedback resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R3	Charging limit resistor	10 Ω 1% 0805 125mW	Vishay	CRCW080510R0FKEA	OneCall	1469859	0.024
R4	Peak hold leak resistor	100 MΩ 1% 0805 125mW	Vishay	CRCW0805100MJPEAHR	OneCall	2395992	0.343
R5	Output series resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R6	Output shunt attenuator resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R7	Reset pull-down resistor	100 kΩ 1% 0805 125mW	Vishay	CRCW0805100KFKEA	OneCall	1469860	0.024
R8	Input pull-down resistor	10 MΩ 1% 0805 125mW	Vishay	CRCW080510M0FKEA	OneCall	1469858	0.028
VR1	Offset adjust trimpot	10 kΩ trimmer12 turns, 3266 series, 250 mW, ± 10%	Bourns	3266W-1-103LF	OneCall	9352651	3.88
C1	Input low pass filter capacitor	1 nF 0805, 50V, 50 V, X7R	AVX	08055C102JAT2A	OneCall	1833879	0.148
C2	Input clamp capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C3	U1 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C4	U2 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C5	U1 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C6	U2 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C7	Peak hold capacitor	10 nF 63V - Polystyrene, 10000 pF, 63 V, ± 1%, FSC/EX Series	LCR Components	FSCEX 10000PF 1% 63V	OneCall	9520414	1.81
Cf	Feedback stabilising capacitor	150 pF, 50 V, 0805 [2012 Metric], ± 5%, C0G / NP0, VJ Series		VJ0805A151JXACW1BC	OneCall	2896481	0.0325
						TOTAL	**35.22**

Version D

ID	Item	Description	Manufacturer	Model #	Supplier	Part #	Total
--	Printed circuit board Double-sided	Filename: Peak detector module.pcb	Gray		Beta Layout	---	9.11
CN1	DC power input header	8 way Molex 0.1" right angle	Molex	22-05-2081	OneCall	9731237	0.572
U1	Input operational amplifier,	Single, 79.9 MHz, 170 V/µs, ± 5V to ± 15V, SOI- 8	Analogue Devices	ADA4637-1ARZ	OneCall	2067786	6.51
U2	Output operational amplifier	41 MHz, 140 V/µs, ± 5V to ± 15V, SOIC-8	Analogue Devices	AD825ARZ	OneCall	9603735	4.07
U3	Clamp analogue switch	SPST, 1 channels, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
U4	Reset analogue switch	SPST, 1 channels, 200 ohm, ± 5V to ± 16.5V, SOT-23- 6	Analogue Devices	ADG1201BRJZ-R2	OneCall	2409934	2.79
D1	Negative clamp diode	Small signal diode, single, 75 V, 150 mA, 1 V, 4 ns	Taiwan Semi	TS4148 RYG	OneCall	2708389	0.036
D2	Peak charging diode	Small signal diode, 150 V, 200 mA, 1.15 V, 1 A, low leakage	On Semiconductor	FDH333	OneCall	9843760	0.17
R1	Input low pass filter resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R2	Feedback resistor	1 kΩ 1% 0805 125mW	Vishay	CRCW08051K00FKEA	OneCall	1469847	0.048
R3	Charging limit resistor	10 Ω 1% 0805 125mW	Vishay	CRCW080510R0FKEA	OneCall	1469859	0.024
R4	Peak hold leak resistor	100 MΩ 1% 0805 125mW	Vishay	CRCW0805100MJPEAHR	OneCall	2395992	0.343
R5	Output series resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R6	Output shunt attenuator resistor	5.1 kΩ 1% 0805 125mW	Vishay	CRCW08055K10FKEA	OneCall	1469937	0.027
R7	Reset pull-down resistor	100 kΩ 1% 0805 125mW	Vishay	CRCW0805100KFKEA	OneCall	1469860	0.024
R8	Input pull-down resistor	10 MΩ 1% 0805 125mW	Vishay	CRCW080510M0FKEA	OneCall	1469858	0.028
VR1	Offset adjust trimpot	10 kΩ trimmer12 turns, 3266 series, 250 mW, ± 10%	Bourns	3266W-1-103LF	OneCall	9352651	3.88
C1	Input low pass filter capacitor	1 nF 0805, 50V, 50 V, X7R	AVX	08055C102JAT2A	OneCall	1833879	0.148
C2	Input clamp capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C3	U1 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C4	U2 +ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C5	U1 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C6	U2 -ve supply decoupling capacitor	100 nF, 50 V, ± 5%, X7R	AVX	08055C104JAT2A	OneCall	1740673	0.034
C7	Peak hold capacitor	10 nF 63V - Polystyrene, 10000 pF, 63 V, ± 1%, FSC/EX Series	LCR Components	FSCEX 10000PF 1% 63V	OneCall	9520414	1.81
Cf	Feedback stabilising capacitor	150 pF, 50 V, 0805 [2012 Metric], ± 5%, C0G / NP0, VJ Series		VJ0805A151JXACW1BC	OneCall	2896481	0.0325
						TOTAL	**32.66**

9. Conclusion

The approaches described here are not particularly novel but show that it is readily possible to implement pretty reasonably-performing peak detector in the analogue world. Some of the operational amplifiers are either obsolete or fast becoming so, so in the future we would be using the ADA4637 + ADA4627 combination (version C). It is essential that a high slew rate, wide bandwidth amplifier is used as the first stage and a low input bias current amplifier is used for the second stage. Doubtless in the future we may redesign the board for different packages but unfortunately the trend points towards lower supply voltage operational amplifiers that inevitably degrade the dynamic range somewhat. Attention should be paid to the choice of hold capacitor and charging diode and these should be chosen for the application in hand. But hey, there are lots of applications!

This note was prepared in September 2015 by B Vojnovic and RG Newman, who also constructed the unit, and performed testing along with B Vojnovic. Thanks to S Fry for data plotting and to IDC Tullis for useful comments.

The financial support of Cancer Research UK, the MRC and EPSRC is gratefully acknowledged.